Core overview

The jesd ip comprises 4 files :

- define_jesd204b.v
- jesd204b_reg_mngt.v
- jesd204b_tx.v
- jesd204b_tx_wrapper.v

jesd204b_tx_wrapper is the top level.

The goal of this ip is to replace, in the veriqloud context, the logicore ip jesd204c from xilinx.

Only Tx 204b is supported.

Parameter description

NAME	TYPE	VALUE	DESCRIPTION
C_s_axil_DATA_WIDTH	integer	32	Axi-Lite data width
C_s_axil_ADDR_WIDTH	integer	12	Axi-Lite address width
C_L	integer	4,1	Lane number

Ports description

NAME	Interface	I/O	DESCRIPTION
tx_core_clk	System s_axis_tx	I	Core logic clock input. Frequency: Serial line rate / 40 (for 8B10B linecoding
tx_core_reset	System	I	Core asynchronous logic reset active-High.
s_axil_aclk	s_axil	I	AXI4-Lite clock input.
S_axil*	s_axil		AXI4-Lite
s_axil_aresetn	s_axil	I	AXI4-Lite reset input. Active-Low.
btx_sysref_i	System	I	SYSREF input.
btx_sync_i	System	I	Sync signal. The sync signal is defined as an active-

			Low sync request signal by JESD204 so this signal is Low until comma alignment is completed and High to request ILA and normal data
btx_reset_gt_o	System	O	JESD204_PHY TX datapath reset. Core output to reset the transmit datapath in a connected JESD204_PHY. This must be connected to a JESD204_PHY.
btx_reset_done_i	System	I	JESD204_PHY TX reset done input. Indicates the JESD204_PHY has completed the transmit reset process.
vgtN_tdata_o[31:0]	PHY	O	TX data to JESD204 PHY. N = 4. If c_L = 1 only vgt0_tdata_o used. The other ones are stucked at 0.
vgtN_charisk_o[3:0]	PHY	O	TX Char is K to JESD204 PHY. N = 4. If c_L = 1 only vgt0_charisk_o used. The other ones are stucked at 0
vtx_tdata_i [(32*N)-1:0]	s_axis_tx	I	Transmit data input. N=c_L
btx_tready_o	s_axis_tx	O	AXI4-Stream tready

Registers space

AXI4-Lite Address	Register name
0x024	CTRL_ENABLE
0x034	CTRL_SUBCLASS
0x03C	CTRL_8B10B_CFG
0x050	CTRL_SYSREF
0x070	CTRL_TX_ILA_CFG0
0x074	CTRL_TX_ILA_CFG1
0x078	CTRL_TX_ILA_CFG2
0x07C	CTRL_TX_ILA_CFG3
0x404	CTRL_TX_ILA_LID

CTRL_ENABLE

Bits	Default version	Description
1	0	Enable Data Interface. 1 = Enables the AXI4-Stream Data interface and

		transmits/receives data on the link. 0 = The link will be transmitting/receiving 0s

CTRL_SUBCLASS

Bits	Default version	Description
1 :0	0	Sub Class: 1 = Subclass 1

CTRL_8B10B_CFG

Bits	Default version	Description
31:24	0	ILA multiframes. Multiframes in the Transmitted Initial Lane Alignment Sequence. Parameter Range: 4–256; program the register with required value minus 1
12 :8	0	Frames per Multiframe (K) Parameter range 1–32; Program register with required value minus 1 (for example, for K = 16, 0x0F should be programmed)
7 :0	0	Octets per Frame (F) Parameter range 1–256; Program register with required value minus 1 (for example, for F = 4, 0x03 should be programmed)

CTRL_SYSREF

Bits	Default version	Description
1	0	SYSREF Required on Re-Sync 1 = Following a Link Re-Sync event, a SYSREF event is required to re-align the local LMFC/LEMC before the link will operate. 0 = No SYSREF is required to restart a link after a Re-sync event.
0	0	SYSREF Always 1 = The core will align the LMFC/LEMC counter on all SYSREF events. 0 = The core will only align the LMFC/LEMC counter on the first SYSREF event following a reset, all subsequent SYSREF events will be ignored.

CTRL_TX_ILA_CFG0

Bits	Default version	Description
11 :8	0	BID (Bank ID). Binary value.
7 :0	0	DID (Device ID). Binary value

CTRL_TX_ILA_CFG1

Bits	Default version	Description
25 :24	0	CS (Control bits per Sample). Binary value.
20 :16	0	N' (Totals bits per Sample). Binary value minus 1.
12 :8	0	N (Converter Resolution). Binary value minus 1.
7 :0	0	M (Converters per Device). Binary value minus 1.

CTRL_TX_ILA_CFG2

Bits	Default version	Description
28 :24	0	CF (Control Words per Frame). Binary value.
16	0	HD (High Density format)
12 :8	0	S (Samples per Converter per Frame). Binary value minus 1

CTRL_TX_ILA_CFG3 : Set to 0

CTRL_TX_ILA_LID

Bits	Default version	Description
20 :16	0	Number of lanes per link (binary value minus 1).
4 :0	0	ID of lane 0. Value can be anywhere between 0 and 31. ID of lane 1 equal at Id of lane 0+1… ID of lane 3 equal at Id of lane 0+3

Integration :

Default configuration to send by axi4-lite after power on (I simulated it)

AXI4-Lite register address	AXI4-Lite register data
00000034	00000001

0000003c	03021f00
00000050	00000003
00000070	0000071f
00000074	000f0f01
00000078	00010000
0000007c	00000000
00000404	00030000
00000024	00000002

Timing error.

When I launched a synthesis,there was some timing violations on axi_interconnect_0 module in fastdac diagram. To fix them I enabled data fifo (32deep) on master interface. Doublle click on module, then selects Master interface then set property.

Constraint file.

In the xdc constraints file of FPGA_TURNKEY project you must add the following constraint :

- set_false_path -through [get_pins FPGA_TURNKEY*/FASTDAC_wrapper/fastdac_tx_core_reset] -to [get_pins FPGA_TURNKEY*/FASTDAC_wrapper/inst/FASTDAC*/*wrapper/*/*vtx_reset_gt*/PRE]

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You have to update LFMCDEL and LMFCVAR parameters